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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,737	05/09/2002	Jimmy Hsu	8727-US-PA	6244

31561 7590 06/10/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
BOWERS, BRANDON	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,737	HSU, JIMMY	
	Examiner	Art Unit	
	Brandon W Bowers	2825	

-- Th MAILING DATE of this communication appears on th cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sharma et al, US Patent No. 5,990,547.

In reference to claim 16, Sharma teaches a multi-layered substrate having a voltage reference signal circuit layout therein (Figure 1 and column 3 line 53 – column 4 line 19) comprising at least one signal layer having a plurality of signal traces (column 3, lines 54-55), a non-signaling layer having a voltage reference signal trace (column 3, lines 55-56), and a conductive plane between the signal layer and the non-signal layer (column 3, lines1-13).

In reference to claim 17, Sharma teaches wherein the non-signaling layer includes at least one power plane (column 3, lines 53-57).

In reference to claim 18, Sharma teaches wherein the non-signaling layer includes at least one ground layer plane (column 3, lines 53-57).

In reference to claim 19, Sharma teaches wherein the non-signaling layer includes at least one power plane and a plurality of signal traces (column 3, lines 57-column 4, line 19).

In reference to claim 20, Sharma teaches wherein the non-signaling layer includes at least one ground layer plane and a plurality of signal traces (column 3, lines 57-column 4, line 19).

In reference to claim 21, Sharma teaches wherein the conductive plane includes a ground plane (column 3, lines1-13 and 55-57).

In reference to claim 22, Sharma teaches wherein the conductive plane includes a power plane (column 3, lines1-13 and 55-57).

Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Honsinger et al., US Patent No. 5,500,804.

In reference to claim 16, Honsinger teaches a multi-layered substrate having a voltage reference signal circuit layout therein comprising at least one signal layer having a plurality of signal traces, a non-signaling layer having a voltage reference signal trace, and a conductive plane between the signal layer and the non-signal layer (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 17, Honsinger teaches wherein the non-signaling layer includes at least one power plane (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 18, Honsinger teaches wherein the non-signaling layer includes at least one ground layer plane (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 19, Honsinger teaches wherein the non-signaling layer includes at least one power plane and a plurality of signal traces (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 20, Honsinger teaches wherein the non-signaling layer includes at least one ground layer plane and a plurality of signal traces (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 21, Honsinger teaches wherein the conductive plane includes a ground plane (Figure 1 and column 3 line 64 – column 4 line 33).

In reference to claim 22, Honsinger teaches wherein the conductive plane includes a power plane (Figure 1 and column 3 line 64 – column 4 line 33).

Response to Arguments

Applicant's arguments filed 19 March 2004 have been fully considered but they are not persuasive. Applicant argues that neither Sharma nor Honsinger teach a non-signaling layer having a voltage reference signal trace. Both Sharma and Honsinger teach voltage reference layer. These are non-signaling layers made up entirely of voltage reference signal traces. Accordingly, both Sharma and Honsinger teach a non-signaling layer having a voltage reference signal trace.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., reducing/preventing interference between a voltage reference signal trace and other signal traces) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BWB

LEIGH M. GARBOWSKI
PRIMARY EXAMINER